A Design Methodology using Flip-Flops Controlled by PVT Variation Detection

Alexandro Giron-Allende, and Victor Avendaño
Freescale Semiconductor
Guadalajara, Mexico
Alex.Giron@freescale.com
Victor.Avendano@freescale.com

Esteban Martinez-Guerrero
Department of Electronics Systems and Informatics
ITESO-The Jesuit University of Guadalajara
Guadalajara, 45604, Mexico
margres@iteso.mx

***Abstract*— A design methodology for sequential logic circuits using controllable flip-flops is proposed. The flip-flop setup time and propagation delay is controlled with a process, voltage and temperature (PVT) detector using an additional setup time and delay control (SDC) input. With this SDC enable, it is possible to enhance the circuit timing performance when PVT variations are detected. The PVT detector is based in the propagation delay of digital buffers. When an increase in the propagation delay is detected in the digital logic, the SDC flip-flop input is enabled to reduce its setup time and Clk-Q propagation delay. When the PVT conditions are maintained under the selected threshold, the SDC control remains disabled, saving power. The proposed flip-flop and PVT detector are designed and characterized in a TSMC 28 nm bulk CMOS technology.**

Keywords*— *CMOS sequential circuits; flip-flop; setup time; controllable; PVT; low power; high speed.

I. INTRODUCTION

Modern communication microprocessors are constantly demanding a faster data processing [1]. Looking for methodologies to allow circuits to operate at higher frequencies and improve their power management became an important challenge [2]. Digital circuits timing optimization is one of the main aspects to consider in these improvements. Process, voltage and temperature (PVT) variations affect many characteristics of CMOS circuits, such as the propagation delay, making the timing optimization more complex. In order to deal with the combination of speed increase and PVT variations, the designer has to consider higher margins of operation to guarantee a correct performance in the critical conditions.

Digital sequential systems are based on the interaction of combinational logic and flip-flops, hence flip-flops are important to determine the area, speed, and power consumption. A basic timing path in a sequential circuit considers the data coming out from a launching flip-flop, passing through combinational logic and being captured by a second flip-flop [1]. From this timing path analysis the following relationship is used to estimate the maximum clock (Clk) frequency that can be achieved,

$$T_c > t_{pcq} + t_{pd} + t_{setup} \quad (1)$$

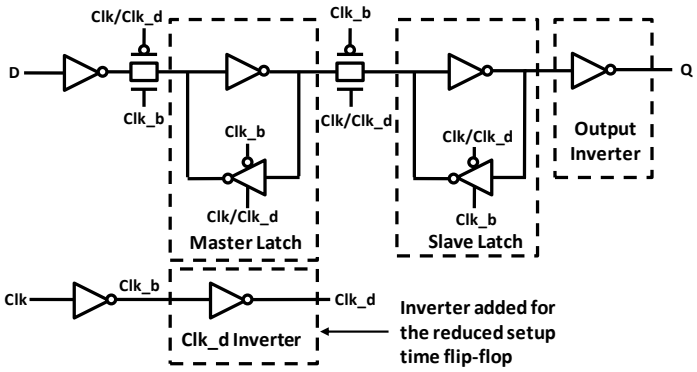

Fig. 1. Conventional master slave Flip-flop architecture

where T_c is the clock period, t_{pcq} is the flip-flop Clk-Q propagation delay, t_{pd} is the combinational logic propagation delay and t_{setup} is the flip-flop setup time (D-Clk delay). From this equation it can be determined that any reduction on the flip-flop setup time or Clk-Q delay allows a clock period reduction and with this a higher operation frequency.

The technology and supply voltage are being scaled down, making circuits more sensitive to PVT variations. Then, techniques robust to variations are becoming necessary to improve the circuit performance and avoid functional failures [3]. Different methodologies have been proposed to minimize the performance lost due to PVT variations, allowing systems to tolerate worst case scenarios [4]. Some of these techniques rely on sensing the process, voltage and temperature individually to adjust the circuit conditions [5]. Separated detectors provide more precise measurements and control but require more area and power consumption.

In this work, a comparative study of a conventional master slave flip-flop and a controllable flip-flop is presented. Timing and power are analyzed and verified through accurate circuit simulations. A PVT detector solution is presented and characterized. Finally, the controllable flip-flop and the PVT detector are tested together on a circuit application to analyze its performance.

This work was supported by CONACYT (*Consejo Nacional de Ciencia y Tecnología, Mexican Government*) under scholarship granted to A. Girón-Allende

978-1-4799-8332-2/15/$31.00 ©2015 IEEE

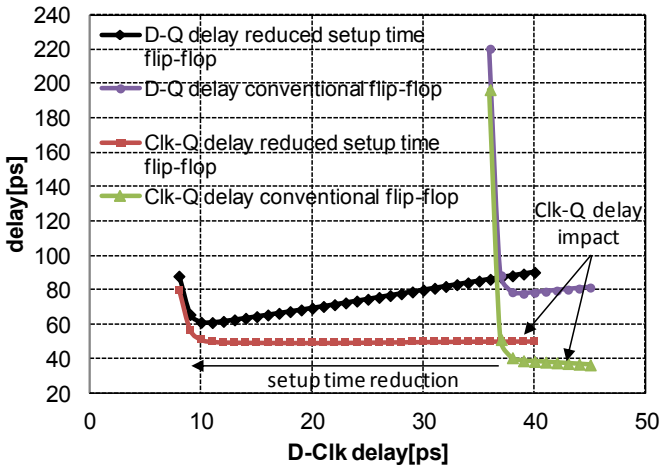

Fig. 2. Conventional master slave Flip-flop setup time curves with and without reduced setup time.

II. Conventional Master slave Flip-flop Characterization

A conventional master slave flip-flop taken from a TSMC 28 nm bulk CMOS standard cell library is used as the reference design (Fig. 1). Some authors have proposed different variations to the conventional master slave flip-flop in order to reduce the setup time [6]. Some of these approaches increase the Clk delay internally by adding inverters and taking different delayed Clk phases for the master and slave flip-flop latches. Nevertheless, this setup reduction has an impact on the Clk-Q delay, adding a trade off to the improvement. A conventional master slave flip-flop is characterized with two architecture variations: using Clk and Clk_b without an additional Clk_d inverter (conventional flip-flop) and using Clk_b and Clk_d with the Clk_d inverter (reduced setup time flip-flop). The setup time (D-Clk delay), Clk-Q and D-Q delays are obtained (Table I). For the flip-flop characterizations presented here, the minimum D-Q delay metric is used for comparison due to its timing performance focus [7]. The setup time curves of the conventional and reduced setup time flip-flops are plotted together (Fig. 2). From these results, it can be confirmed that there is a setup time and D-Q delay reduction in the flip-flop using the Clk_d inverter. However, this setup time reduction comes with a Clk-Q delay increase (Fig. 2, Table I) that could minimize the D-Q improvement and produce a power consumption increase.

III. Setup Time and Clk-Q Delay Reduction Solution

One option to compensate the Clk-Q delay impact caused by the setup time reduction is to increase the strength of the output inverter that provides the Q output. This causes an additional power consumption to the one already caused by the inverter added to the clock path for setup time reduction. The flip-flop performance on a sequential circuit has not always the same speed requirements and is not always working under the same PVT variations.

TABLE I. FLIP-FLOPS CHARACTERIZATION RESULTS

Flip-Flop	Min. setup time D-Clk delay[ps]	Min. Clk-Q delay [ps]	Min. D-Q delay[ps]	Total power [uW]
Conventional	38	40.41	78.56	40.16
Conventional Reduced Setup time	11	49.88	60.88	59.68
Controllable SDC = 0	33	52.73	85.73	46.22
Controllable SDC = 1	10	51.62	61.62	69.79

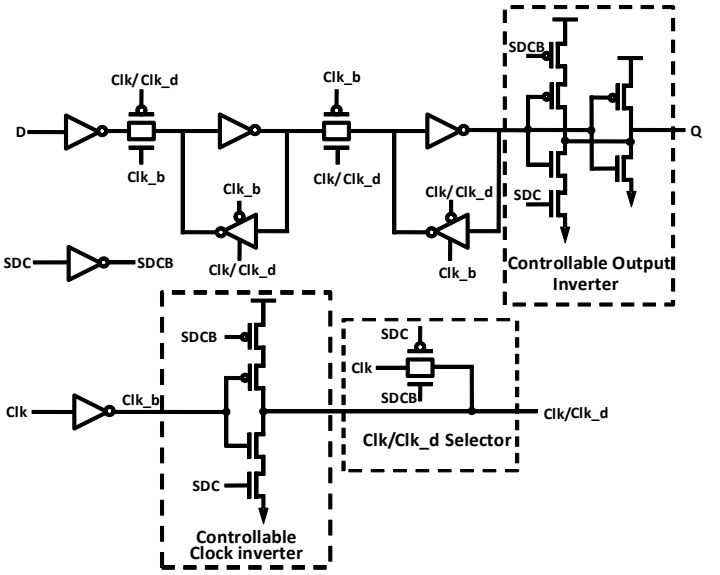

Fig. 3. Controllable flip-flop architecture

The methodology presented in this paper it is based on the idea of reducing the flip-flop setup time together with increasing the flip-flop output inverter strength but only when the PVT conditions produce an increase on the logic circuits delays. Since these stages increase the power consumption and are not always required for all the operating conditions, the capability to select these enhancements leads to the use of a controllable flip-flop.

IV. Controllable Flip-flop Characterization

The controllable flip-flop architecture (Fig. 3) is based on the conventional master slave architecture adding three additional blocks: a controllable output inverter, a controllable clock inverter and a Clk/Clk_d selector. The controllable output inverter consists of two inverters in parallel with one of them controlled with the SDC signal. When the SDC signal is high, both inverters work together, providing more current and reducing the propagation delay Clk-Q. The controllable clock inverter connects a second inverter stage in the clock path only when SDC is high. This extra inverter generates the delayed clock Clk_d. The Clk/Clk_d selector provides the Clk_d signal to control the master and slave latches if SDC is high and provides Clk when SDC is low through a transmission gate. A controllable flip-flop is implemented using the same transistor sizes of the conventional master slave flip-flop by only adding the additional stages described.

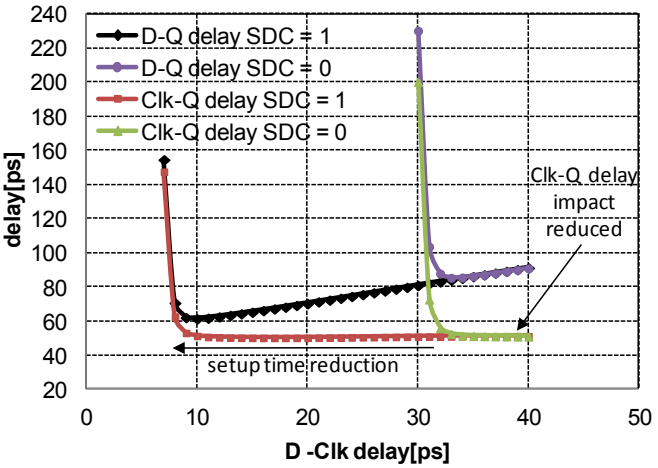

Fig. 4. Controllable flip-flop setup time curves, SDC = 0 and SDC = 1.

The controllable flip-flop is characterized under the same conditions than those used for the conventional and reduced setup time flip-flops to compare the setup time, Clk-Q and D-Q delays when SDC is low and high (Table I, Fig. 4). It can be seen that when SDC is low, there is no reduction on the delays compared to the conventional flip-flop since the extra stages are disabled. In a similar way, when SDC is high the delay is higher in comparison with the reduced setup time flip-flop. Nevertheless, the timing improvement is observed when SDC is high, and the setup time, Clk-Q and D-Q delays are reduced compared with the condition when SDC is low and compared also with the conventional flip flop delays. With this timing improvement there is a power consumption increase that is around 50% compared with the SDC low condition and 17% compared with the reduced setup time flip-flop. The controllable flip-flop requires 40% more transistors compared with the conventional one, representing an area increase.

V. PVT Detector

The PVT detector (Fig.5) is based on the propagation delay variation using an inverter chain to form a delay line and a two flip-flop synchronizer. The clock signal Clk is connected to the flip-flop FF1 clock and also passed through the delay line to have a delayed version at D1. The delay line senses the propagation delay effect on the digital logic due to PVT variations. When the propagation delay in the delay line is under the selected threshold, at the positive edge of Clk, a logic 0 will be present at the D1 input, then captured and propagated to Q1 and at the next Clk cycle to Q2 (delay detection output). This indicates that there is not a high delay condition for that PVT case. When the combination of temperature, voltage and process produces a significant delay increase on the delay line, a logic 1 is present at D1 and propagated to Q2, indicating that a significant change on PVT has been detected in the digital circuits. FF2 is used to minimize the failure probability caused by the possible metastability when the circuit is around the detection threshold. This detector is not intended to sense if the variation is coming from Process, Voltage or Temperature separately; it is detecting the effect of the combined variables. A timing diagram of the PVT detector showing the low and high delay conditions is shown in Fig. 6. The design of the delay detector should meet the following design constraints through the different PVT cases in order to operate correctly:

$$Max.\ delay\ for\ no\ detection = T_c/2 + t_{hold} \quad (2)$$

$$Max.\ delay\ for\ correct\ detection = T_c - t_{setup} \quad (3)$$

where T_c is the clock period, t_{hold} is the flip-flop hold time and t_{setup} is the flip-flop setup time. The number of inverters (stages) in the delay line adjust the desired detection threshold.

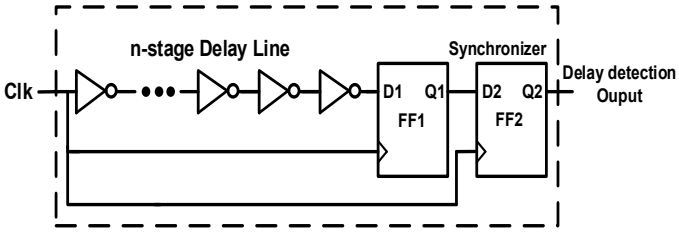

Fig. 5. PVT detector

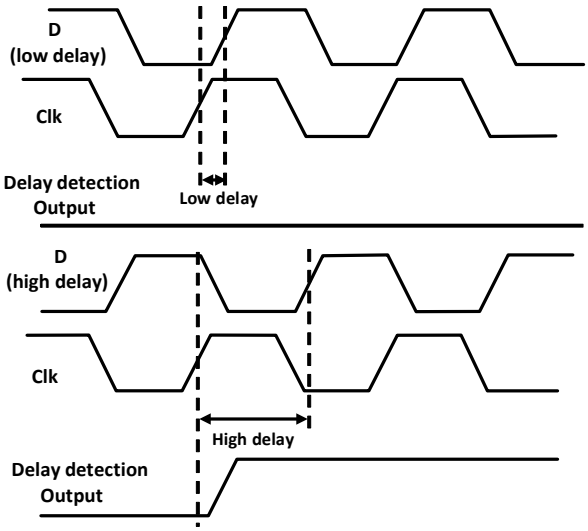

Fig. 6. PVT detector timing diagram for low and high delay detection.

The PVT detector is designed and characterized to work under the following conditions: -40°C, 27°C and 125°C; ff(fast fast) typ(typical) and ss(slow slow) process; 0.9V, 1V and 1.1V supply voltages. The characterization results (Fig. 7) show the propagation delay of the delay line corresponding to different PVT cases and the detector output to indicate the conditions where a high delay on logic circuits is detected. The PVT detector threshold is designed in this case to detect half of all the PVT cases used in the characterization where the delay line shows highest propagation delays, but the threshold can be designed depending of the application.

VI. Controllable Flip-flop Methodology using PVT Detection.

The proposed methodology consists of connecting together the controllable flip-flops with a PVT detector (Fig. 8). A single PVT detector output is used to control the SDC inputs of the flip-flops inside a clock domain.

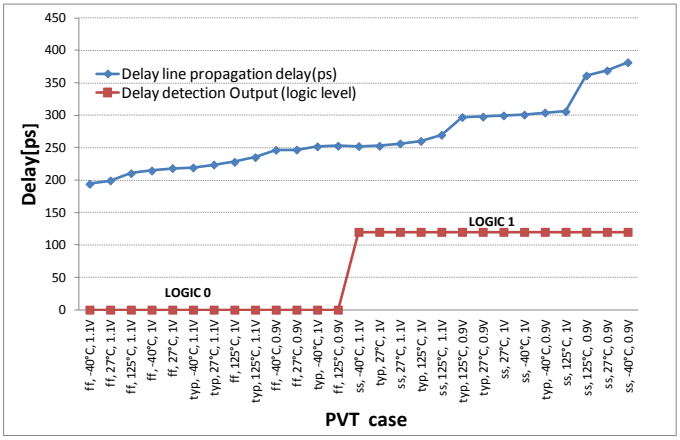

Fig. 7. PVT detector delay line characterization and delay detector output.

The PVT detector circuit senses the propagation delay variation of the logic cells (represented by the delay line) due to the different conditions and enables or disables the SDC signals. When the PVT detector indicates that the propagation delay on the logic has increased more than the expected threshold, the controllable flip-flops will reduce its setup time and Clk-Q propagation delay. When the delay detected is under the threshold, the setup and propagation delay time increase but the power consumption is reduced. With the inclusion of a multiplexer, the PVT output can be overridden to directly control the SDC input. Different detectors can be used on different chip regions to consider intra-chip variations.

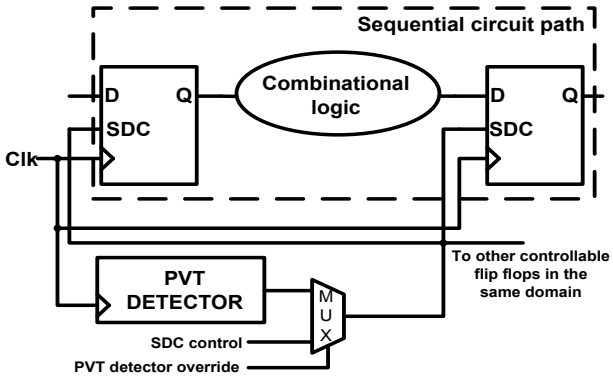

Fig. 8. Design methodology using controllable flip-flops.

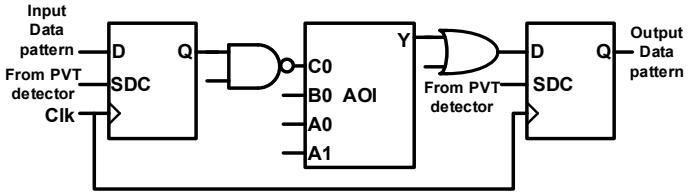

Fig. 9. SerDes circuit timing path.

VII. Simulation Results

A controllable flip-flop and a PVT detector are designed and tested in a path taken from a PLL digital feedback divider used on a high speed SerDes (Serializer/Deserializer) circuit (Fig. 9). The circuit is simulated at different frequencies and PVTs using the expected input data pattern.

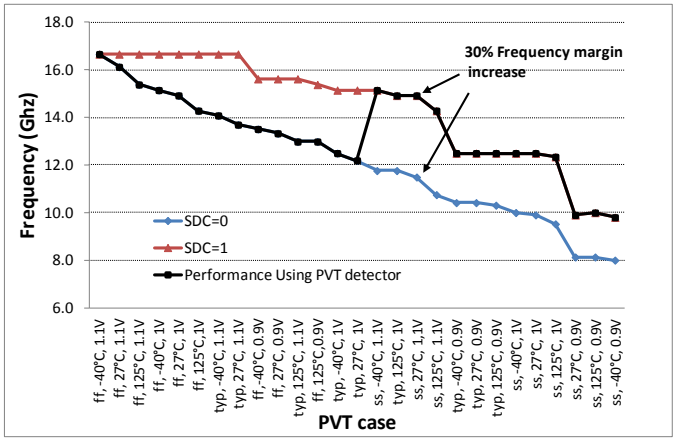

Fig. 10. SERDES circuit timing path simulation results.

From the results shown in Figure 10, it is observed that when the PVT detector senses a propagation delay increase on the logic circuits the frequency margin is improved up to 30%, providing more time margin to the circuit.

VIII. Conclusion

With the presented design methodology, sequential CMOS circuits increase automatically its frequency response when are working on PVT conditions that increase the propagation delay, and reduce their power consumption when high delay conditions are not present. The PVT detector presented here senses PVT changes providing a control signal to controllable flip-flops. The conventional flip-flop characterizations showed that the timing improvement gained with the setup reduction has an impact on the Clk-Q and D-Q delays. The proposed controllable flip-flop showed a timing improvement compared with the conventional and reduced setup time flip-flops. This improvement comes with power and area trade off. The results shown on a circuit application confirmed that the design methodology provides significant timing improvements. This methodology could reduce the static timing adjustment effort by giving and additional timing margin in some PVTs.

References

[1] V.G. Oklobdzija, "Multi-GHz Systems Clocking," in *Proceedings of IEEE Int. Conf. on ASIC*, Beijing, China, Oct. 2003, pp. 701-706.

[2] M. Nakai et al., "Dynamic Voltage and Frequency Management for a Low-Power Embedded Microprocessor," in *IEEE Journal of Solid-State Circuits*, vol.40, pp. 28-35, Jan. 2005.

[3] D. Wolpert, and P. Ampadu,"A Low-Power Safety Mode for Variation Tolerant Systems-on-Chip," in *IEEE Int. Symp. on Defect and Fault Tolerance of VLSI Systems*, Boston, MA., Oct 2008, pp. 33-41.

[4] M.-H. Chang et al., "Near-/Sub-Vth Process, Voltage, and Temperature (PVT) Sensors with Dynamic Voltage Selection," in *IEEE Int. Symp. On Circuit and Systems (ISCAS)*, Beijing, China, May 2013, pp.133-136.

[5] S.-W. Chen, M.-H. Chang, W.-C. Hsieh, and W. Hwang, "Fully On-chip Temperature, Process, and Voltage Sensors," in *IEEE Int. Symp. On Circuit and Systems (ISCAS)*, Paris, France, May 2010, pp.897-900.

[6] J. Zhou, J. Liu, and D. Zhou, "Reduced setup time static D flip-flop," Electronics Letters, vol. 37, pp 279-280, March 2001.

[7] V. Stojanovic, V.G. Oklobdzija, and R. Bajwa, "A Unified Approach in the Analysis of Latches and Flip-Flops for Low-Power Systems," in *IEEE Int. Symp. On Low Power Electronics and Design,* Monterey, CA., Aug. 1998, pp. 227-232.