CMOS Amplifier with Self-correction Offset for SERDES Applications

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Abstract: In Serializer/Deserializer (SERDES) systems usually there is a mismatch between the devices used in the circuitry handling the two complimentary signals and the analog front-end equalizer (AFE) circuit that introduce an unknown and relatively slowly varying offset voltage into the differential signals, this offset affects the noise margin of the system. A design of self-correction offset amplifier based on a continuous-time closed loop self-correction offset system is proposed for minimizing various possible offsets coming from input or from differential amplifiers in the range of – 30 mV to + 30 mV. Simulation results shown offset correction at the output of amplifier which allows high speed operation in the SERDES system. The amplifier was designed in AMI 0.5 µm CMOS technology, for 6 mW of power consumption and 3.0 V supply.

***Keywords*—**MOS integrated circuits, analog circuits, differential amplifiers, low-pass filters, circuit simulation, offset correction,

I. Introduction

Input-referred offset voltage is one the most important drawbacks of MOS analog circuits when compared to their BJT or BiCMOS counterparts. Typically the offset voltage ranges from 10 mV to 30 mV [1, 2]. Offset voltage can be caused by unbalanced input from preceding stages or by device mismatch in the amplifier itself [3]. Without offset cancellation circuitry, the introduced DC offset might saturate the amplifier output stage which in turn can reduce the amplifier dynamic range and then prohibits the amplification of the desired signal. This problem is even worse in low-supply applications. Traditional dynamic offset cancellation techniques such as auto-zeroing and others, usually utilize sampling circuit and memory components to sample, store and cancel the offset voltage [1, 4]. The main disadvantages with these methods are that they require a clock signal and a calibration period. A clock signal would cause problems with clock feedthrough and charge injection, which make cancellation inaccurate. On the other hand, the calibration period would reduce the overall speed and prevent the amplifier to operate in a continuous-time way, unless the ping-pong architecture is used [2, 5]. For continuous-time amplifiers main offset cancellation techniques reported in literature are: (1) Chopping [6, 7], (2) Inter-stage and/or input AC coupling high pass filter (HPF) in feedforward path [8, 9], (3) Low pass filter (LPF) [10, 11] or Multi-tap peak detector in feedback path [12], and (4) Feedforward offset cancellation using peak detector [13]. Each technique presents advantages or disadvantages for determined application, for instance, in chopping technique the offset is frequency modulated and removed by a low pass filter, here the filter limits the bandwidth of the amplifier and so this technique is not suitable for high bandwidth applications [14]. Conventional AC coupling technique suffers from area penalty due to large capacitance and resistance requirements to minimize the loss of in-band signal energy. Feedback offset cancellation might not be suitable for high gain amplifiers due to potential stability issues [10, 15] and so on for other techniques.

Differential signaling is widely used in Serializer/Deserializer (SERDES) systems. In an ideal scenario, the circuitry handling the two complimentary signals, are perfectly matched leading to zero offset voltage between the differential signals. In practice, however, there is typically a mismatch between the devices used in the circuitry handling the two complimentary signals and the analog front-end equalizer (AFE) circuit which introduce an

unknown and relatively slowly varying offset voltage into the differential signals [16]. Since the offset voltage is generally a slowly varying signal, its frequency content is typically concentrated near DC. In SERDES system offset voltage affects mainly the noise margin.

This work is focused on the design of a self-correction offset amplifier based on a continuous-time closed loop self-correction offset system. The main purpose of this offset cancellation is to eliminate or minimize various possible offsets coming from input or from differential amplifiers, resulting in minimum remaining offset error at the output without affecting the signal dynamic across the gain stages and allowing high speed operation.

II. Offset correction scheme

Fig. 1 presents a block diagram of the self-correction offset amplifier approach. The circuit has two operating modes: a normal mode when it functions as traditional open loop amplifier and an offset adjusting mode in which the system trims its own offset. The operation mode is enabled/disabled by a control logic circuit. The offset compensation loop is composed by a RC passive low pass filter (LPF), an Operational Transcoductance Amplifier (OTA) working as a difference amplifier, and a simple differential pair working as a transcoductance comparator (TC). The LPF takes the high speed output signals and provides the DC level information from each one. The difference on these levels is generated by the difference amplifier which corresponds to the output offset voltage. This signal is then compared with a reference voltage corresponding to the case of zero offset. The difference on these levels is then converted to current and added to the currents coming from the differential pair from first stage. Since the currents on the differential pair are the voltage to current conversion from the input offset voltage, adding the same current but in opposite direction will produce the correction.

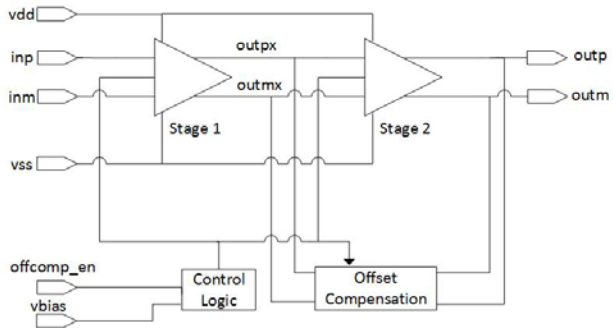

Fig. 1: Block diagram of self-correction offset CMOS amplifier

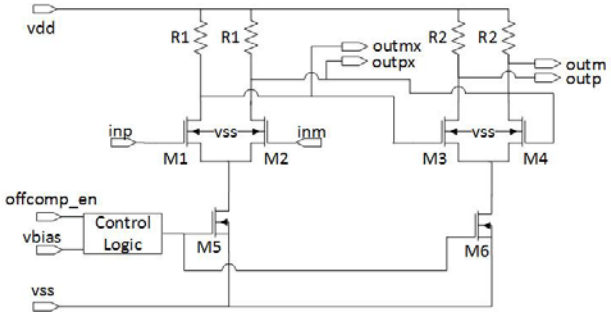

Fig. 2: schematic of CMOS amplifier

Finally, this total current is converted to voltage through the first stage resistors load. This amplifier is part of a SERDES system.

III. Circuit implementation

The detailed circuit implementation of the CMOS amplifier is shown in Fig. 2. The two cell amplifiers are simple differential amplifier with resistive load and cascaded to achieve the desired amplifier gain. The output of first amplifier (A1) consisting of M1 and M2 is sent to the second differential amplifier stages (A2) which consists of M3-M4. The amplifier was designed with parameters of AMI 0.5 µm CMOS process, 6 mW of power consumption and 3.0 V of single rail bias. Calculated values of transistor's size to get 32.6 dB of DC gain and 200 MHz of bandwidth are: W=18.5 µm for M1 and M2 and 16.2 µm for M3 and M4 with L = 1.0 µm for the four transistors, R1 = 2.17 kΩ and R2 = 5.65 kΩ. Use of small differential pairs has the purpose of reducing parasitic and power consumption. The comparator is implemented with a differential pair (M7 to M10) working as a transconductance comparator (Fig. 3). The low pas filter to generate currents for the comparator block is a simple RC filter with cutoff frequency near of 3 MHz which leads to R3 = 50 kΩ, and C1 = 1pfF. The whole detailed circuit is shown in Fig. 3.

Main contribution of DC offset voltage in the gain stage becomes from differential pair and current mirror, then the DC offset voltage (Vos) is determined by adding both contributions. For the differential pair, both inputs are connected to the ground. Since the differential pair is current biased, only a voltage error will be present. On the other hand, since the current mirror is voltage biased, the contribution to the offset voltage will be the current error, so the offset voltage in the cell amplifier is given by Eq. (1) [17]:

$$V_{os} = \left(\frac{A_{VThnMOS}}{\sqrt{WL}}\right)_{1,2} + \frac{(V_{GS}-V_{Th})_1}{(V_{GS}-V_{Th})_5}\left(\frac{A_{VThnMOS}}{\sqrt{WL}}\right)_{5,6} \text{------- (1)}$$

where A_{VTh} is the threshold process area proportionally dependent parameter.

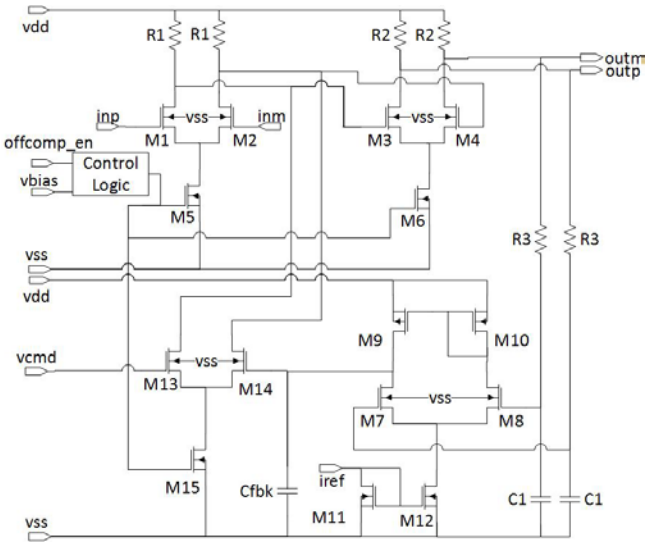

Fig. 3: Detailed schematic of self-correction offset CMOS amplifier

The expected theoretical offset from differential pairs is less than 10 mV, and then assuming the main contribution to the input offset is due to the external input signals.

IV. Simulation results and discussion

AC sweep simulations were performed using Virtuoso-Cadence in order to verify the frequency performance of the amplifier with and without offset correction enabled (Fig. 4). It is clear from Fig. 4 that the amplifier has 32 dB of DC gain and 200 MHz of bandwidth (see solid line in Fig. 4). When the offset corrector loop is disabled, the amplifier response is the traditional low pass type generated by the two DC coupled amplifier stages. On the other hand, when the offset corrector loop is enabled, a low frequency pole is generated by the

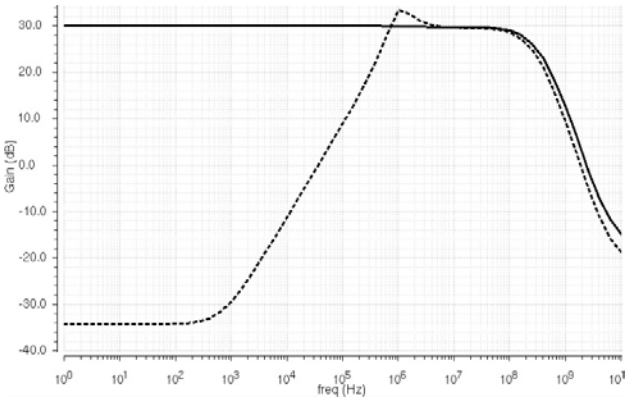

Fig. 4: Simulated AC responses of the amplifier with proposed offset cancellation (open loop DC gain solid line, closed loop DC gain dotted line).

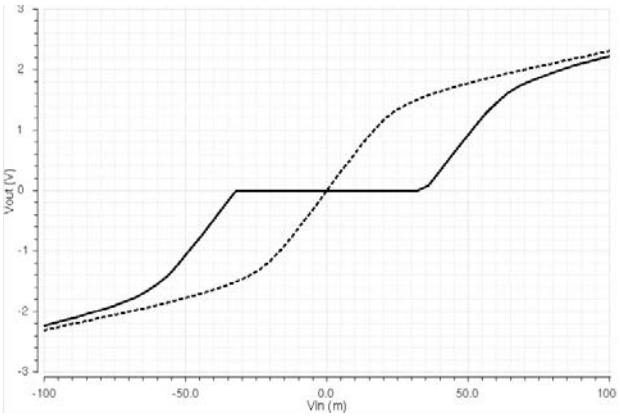

Fig. 5: Offset correction range

feedback OTA working as difference amplifier, generating then a pass-band type frequency response, where it can be appreciated that all the DC and low frequency input components are removed but the high frequency response of the amplifier is preserved.

In order to verify the offset correction range, a DC sweep in voltage was performed (Fig. 5). As can be noticed on Fig. 5, the offset correction range is from -30 mV to +30 mV (see solid line).

To verify the transient response, the amplifier was tested for an input signal ranging from 0 to 10 mV and 10 mV to -10mV (Fig. 6) that emulates input offset coming from preceding stages. As it is observed on Fig. 6, the natural response of amplifier disappear over 1.5 µs which demonstrates the offset cancellation in relatively small time and then the correct operation in the SERDES system is suitable.

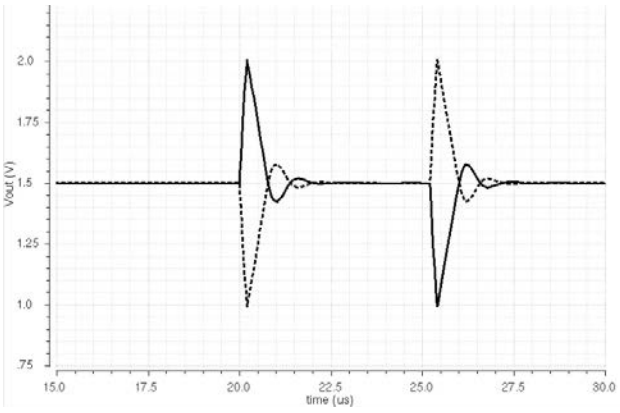

Fig. 6: Transient response of amplifier (outp: solid line, outn: dotted line), showing offset correction in 1.5us.

V. Conclusions

A design of CMOS amplifier with self-correction offset was presented. Simulations results shown the amplifier develops 32.6dB DC gain and 200MHz of bandwidth, a capability to correct disturbances in input signals in the range of -30 mV to + 30mV in a short time (1.5us) These results demonstrate that the offset correction does not affect the signal dynamic across the gain stages and allows high speed operation in SERDES system.

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